# Design and Bandwidth Analysis of Fault-Tolerant Multistage Interconnection Networks 

${ }^{1}$ Rinkle Aggarwal and ${ }^{2}$ Lakhwinder Kaur<br>${ }^{1}$ Department of Computer Science and Engineering, Thapar University, Patiala-147004 India<br>${ }^{2}$ Department of Computer Engineering, Punjabi University, Patiala-147002 India


#### Abstract

The design of a suitable interconnection network for inter-processor communication is one of the key issues of the system performance. In this study a new irregular interconnection network IABN (Irregular Augmented Baseline) has been proposed. IABN is designed by modifying existing ABN (Augmented Baseline Network). ABN is a regular multi-path network with limited fault tolerance. IABN provides three times more paths between any pair of source-destination in comparison to ABN. The ABN and IABN MINs are analyzed and compared in terms of performance parameters namely Bandwidth, Cost and Bandwidth per unit Cost. The proposed network IABN provides much better fault-tolerance and almost double bandwidth at the expanse of little more cost than ABN .


Key words: Multistage Interconnection networks, bandwidth, augmented baseline network, irregular augmented baseline network, fault-tolerance, cost-effectiveness

## INTRODUCTION

Advances in LSI and VLSI technology are encouraging greater use of multiple-processor systems with processing elements to provide computational parallelism and memory modules to store the data required by the processing elements. Interconnection Networks (INs) play a major role in the performance of modem parallel computers. Many aspects of INs, such as implementation complexity, routing algorithms, performance evaluation, fault-tolerance, and reliability have been the subjects of research over the years. There are many factors that may affect the choice of appropriate interconnection network for the underlying parallel computing environment ${ }^{[5,6]}$. Though crossbar is the ideal IN for shared memory multiprocessor, where N inputs can simultaneously get connected to N outputs, but the hardware cost grows astronomically. Multistage Interconnection Networks (MINs) are recognized as cost-effective means to provide programmable data paths between functional modules in multiprocessor systems. These networks are usually implemented with simple modular switches, employing two-input two-output switching elements. Most of the MINs proposed in the literature have been constructed with $2 \times 2$ crossbar switches as basic elements, and have $\mathrm{n}=\log _{2} \mathrm{~N}$ switching stages with each stage consisting of N/2 elements, which makes the cost of this network as $\mathrm{O}(\mathrm{N} \log \mathrm{N})$, as compared to $\mathrm{O}\left(\mathrm{N}^{2}\right)$ for a crossbar ${ }^{[4]}$. The pattern of interconnection may be uniform or nonuniform, which classifies the MINs to be regular or
irregular respectively ${ }^{[7]}$. In the case of irregular networks, the path length varies from any input to any output, in contrast with regular networks, where it is the same ${ }^{[10]}$. Fault-tolerance in an interconnection network is very important for its continuous operation over a relatively long period of time ${ }^{[8]}$. Fault-tolerance is the ability of the network to operate even in the presence of faults, although at a degraded performance. Reliability and other issues related to MINs have also been widely covered, but little attention has been paid to the bandwidth of these networks.

## MATERIALS AND METHODS

Structure and design of networks: ABN (Augmented baseline network): An ABN of size $\mathrm{N} x \mathrm{~N}$ consists of, two identical groups of $\mathrm{N} 2^{-1}$ sources and $\mathrm{N} 2^{-1}$ destinations. The switches in the last stage are of size $2 \times 2$ and the remaining switches in stages 1 through $\mathrm{n}-3$ $\left(\mathrm{n}=\log _{2} \mathrm{~N}\right)$ are of size $3 \times 3{ }^{[9]}$. In each stage, the switches can be grouped into conjugate subsets, where a conjugate subset is composed of all switches in a particular stage that lead to the same subset of destinations. The switches which communicate through the use of auxiliary links form a conjugate loop. The conjugate loops are formed in such a way that the two switches which form a loop have their respective conjugate switches in a different loop. These pair of loops are called conjugate loops ${ }^{[1]}$. Each source is linked to both the groups via multiplexers. An ABN of size $16 \times 16$ is illustrated in Fig. 1.


Fig 1: An ABN of size 16 X 16
Irregular Augmented Baseline Network (IABN): An Irregular Augmented Baseline Network is an augmented baseline network with one additional stage, additional auxiliary links and increased size of demultiplexers. An IABN of size $\mathrm{N} x \mathrm{~N}$ consists of two identical groups of $\mathrm{N} / 2$ sources and $\mathrm{N} / 2$ destinations. Each group consists of a multiple path modified baseline network of size $\mathrm{N} / 2$. The switches in the last stage are of size $2 \times 2$ and the remaining switches in stages 1 through $\mathrm{n}-2\left(\mathrm{n}=\log _{2} \mathrm{~N}\right)$ are of size $3 \times 3$. In each stage, the switches can be grouped into conjugate subsets, where a conjugate subset is composed of all switches in a particular stage that lead to the same subset of destinations. Each source is linked to both the groups via multiplexers. There is one $4 \times 1$ MUX for each input link of a switch in stage 1 and one $1 \times 4$ DEMUX for each output link of a switch in stage n-1. Each group consisting of a modified baseline network of size N/2 plus its associated MUXs and DEMUXs is called a sub network. Thus an IABN consists of two identical sub-networks which are denoted by $\mathrm{G}^{i}$. For example, in Fig. 1, switches A, B, C, D belonging to stage 1 of a subnetwork ( $\mathrm{G}^{\mathrm{i}}$ ) form a conjugate subset, switches A and B form a conjugate pair, and switches A and C form a conjugate loop.

Routing tag for ABN and IABN: A source selects a particular sub network $\left(\mathrm{G}^{1}\right)$ based upon the most significant bit of the destination. Each source is connected to two switches (primary and secondary) in a sub network.
Let the source S and destination D be represented in binary code as:

$$
\begin{aligned}
& \mathrm{S}=\mathrm{s}_{0}, \mathrm{~s}_{1}, \ldots, \mathrm{~s}_{\mathrm{n}-2}, \mathrm{~s}_{\mathrm{n}-1} \\
& \mathrm{D}=\mathrm{d}_{0}, \mathrm{~d}_{1}, \ldots, \mathrm{~d}_{\mathrm{n}-2}, \mathrm{~d}_{\mathrm{n}-1}
\end{aligned}
$$

i. Source $S$ is connected to the $\left(s_{1}, \ldots, \mathrm{~s}_{\mathrm{n}-2}\right)$ primary switch in both the sub-networks through the multiplexers.
ii. Source $S$ is also connected to the $\left[\left\{\left(s_{1}, \ldots, s_{n}\right.\right.\right.$ $\left.\left.\left.{ }_{2}\right)+1\right\} \bmod \mathrm{N} / 4\right]$ secondary switch in both the subnetworks through the multiplexers.

Assumptions: Here are the assumptions on the basis of which the probabilistic relations have been carried out.

- The IN operates in a synchronous mode, i.e., the requests issued by the processors begin and end simultaneously
- The requests are random and the request generated by a processor is independent of the request generated by another processor
- Requests which are not accepted are blocked or rejected
- The requests generated in a cycle are independent of the requests generated in the previous cycle
- " $\mathrm{p}_{0}$ " is the probability with which a processor generates a request. Thus, $\mathrm{p}_{0}$ is the rate of request of a processor per cycle
- The probability with which processor $\mathrm{P}_{\mathrm{i}}$ addresses memory $\mathrm{M}_{\mathrm{i}}$ is zero i.e. there is no favorite memory
- Networks are of same size N x N .


## RESULTS AND DISCUSSION

Bandwith analysis: For calculating probabilistic equations, let us suppose a MIN of size $a^{n} x b^{n}$ with $a^{n}$ sources to $b^{n}$ destinations. The analysis is based on $a x b$ crossbar switches. It is assumed that all the destinations are independently and identically distributed. Let the Request Generation Probability is $p$, at each of the a inputs of a x b crossbar switches. The expected number of requests that passes per unit of time is given by b-b $(1-p / b)^{a}$. Dividing it by number of output lines we get rate of requests at any of the output lines. So output rate, which is function of input line is given by 1-(1-$\left.\mathrm{pb}^{-1}\right)^{\text {a }}$. Since output rate at one stage is input rate to next stage, output rate can be recursively evaluated, starting from initial stage. Output rate of final stage will determine the Bandwidth of a MIN. So Bandwidth BW is
$B W=b^{n} p_{n} \quad$ and $\quad p_{0}=p$.
Probability Equations for $A B N$
$\mathrm{p}[1]=1-(1-\mathrm{p}[0] / 3)^{3}$
$\mathrm{p}[2]=1-(1-\mathrm{p}[1] / 2)^{2}$
Probability Equations for IABN
$\mathrm{p}[1]=1-(1-\mathrm{p}[0] / 3)^{3}$
$\mathrm{p}[2]=1-(1-\mathrm{p}[1] / 6)^{3}$
$\mathrm{p}[3]=1-((1-\mathrm{p}[1] / 2) *(1-\mathrm{p}[2]))^{2}$


Fig. 2: An IABN of size 16 X 16
To have an idea that how these equations have been derived, Consider Fig. 2 of IABN. There are 3 stages. First and last stages have $\mathrm{N} 2^{-1}$ switches whereas middle stage has N/4 switches. As discussed above probability to reach $\mathrm{i}^{\text {th }}$ stage is given by $1-\left(1-\mathrm{p}_{\mathrm{i}-1} \mathrm{~b}^{-1}\right)^{\mathrm{a}}$. In the first stage there are $3 \times 3$ switches, therefore $\mathrm{a}=\mathrm{b}=3$. In second stage, the number of switches is half of the first stage; probability to reach second stage would be half. In last stage, switches are of $2 \times 2$ and the input lines are coming form first and second stages. The number of switches in third stage is double of the second stage and for requests coming from first stage the probability will be same. The results of the Probability equations for Bandwidth are shown in Table 1.

Table 1: Bandwidth of ABN and IABN for different network size

| Probability | Bandwidth |  |
| :---: | :---: | :---: |
| (p) | ABN | IABN |
| 0.1 | 1.509853 | 2.855842 |
| 0.2 | 2.851587 | 5.126124 |
| 0.3 | 4.042236 | 6.93818 |
| 0.4 | 5.097285 | 8.390399 |
| 0.5 | 6.030778 | 9.558997 |
| 0.6 | 6.855424 | 10.503182 |
| 0.7 | 7.582695 | 11.26908 |
| 0.8 | 8.222926 | 11.89273 |
| 0.9 | 8.785405 | 12.402378 |
| 1 | 9.278464 | 12.820238 |


| Table 2: Cost Functions |  |
| :--- | :--- |
| MIN | Cost Functions |
| ABN | $\mathrm{N} / 2\left(3 \log _{2} \mathrm{~N}+13\right)$ |
| IABN | $\mathrm{N} / 2\left(5 \log _{2} \mathrm{~N}+9\right)+9 \log _{2} \mathrm{~N}$ |

Table 3: Cost of ABN and IABN for different network size

| Network Size (LogN) | Cost |  |
| :---: | :---: | :---: |
|  | ABN | IABN |
| 4 | 2.30103 | 2.428135 |
| 5 | 2.651278 | 2.770115 |
| 6 | 2.996512 | 3.114611 |
| 7 | 3.337659 | 3.459242 |
| 8 | 3.675412 | 3.802363 |
| 9 | 4.0103 | 4.143171 |
| 10 | 4.342738 | 4.481414 |

Table 4: Bandwidth per unit cost of ABN and IABN

| Network Size $(\log N)$ | Bandwidth per unit cost |  |
| :--- | :--- | :--- |
|  | ABN | IABN |
| 4 | 3.573585 | 4.897887 |
| 5 | 3.101495 | 4.293225 |
| 6 | 2.744166 | 3.818367 |
| 7 | 2.463681 | 3.437958 |
| 8 | 2.23728 | 3.12772 |
| 9 | 2.050451 | 2.870441 |
| 10 | 1.893488 | 2.653789 |

Cost effectiveness: In this section the MINs are compared on the basis of the cost they incur to interconnect the processors. To estimate the cost of a network it has been assumed that the cost of a switch is proportional to the number of cross-points within a switch. For example a $4 \times 4$ switch has 16 units of hardware cost whereas a $2 \times 2$ switch has 4 units. The cost functions ${ }^{[3]}$ for the various MINs are given in the Table 2 and 3.

Bandwidth per unit cost: Bandwidth per unit cost is obtained by dividing Bandwidth by cost .To make comparison even we fix the request generation probability at $\mathrm{p}=0.8$ and computed the parameter by varying values of N . Higher this parameter better will be the interconnection network (Fig. 3-5). Table 4 shows the Bandwidth per unit cost of ABN and IABN for different network size.

Bandwidth Comparison


Fig. 3: Bandwidth comparison of $A B N$ and IABN


Fig. 4: Cost comparison of ABN and IABN


Fig. 5: Comparison of Bandwidth per unit Cost of ABN and IABN

## CONCLUSION

An Irregular Augmented Baseline Network (IABN) is designed from regular Augmented Baseline Network (ABN) have one extra stage. IABN is a dynamically reroutable and provides multiple paths of varying lengths between a source-destination pair. It has been found that in an IABN, there are six possible paths between any source-destination pair, whereas ABN has only two paths with same length. Thus IABN is more faulttolerant. The Bandwidth analysis shows that IABN has better performance than ABN.

## REFERENCES

1. Aggarwal R., H. Aggarwal and L. Kaur, 2008. On bandwidth analysis of irregular fault-tolerant multistage interconnection networks. Int. Rev. Comput. Software, 3: 199-202.
2. Aggarwal H., and P.K. Bansal, 2002. Routing and Path Length Algorithm for Cost Effective Modified Four Tree Network. IEEE TENCON, pp: 293-294. http://www3.interscience.wiley.com/journal/91513 236/abstract
3. Bansal P.K., R.C. Joshi and K. Singh, 1994. On a fault-tolerant Multi-stage interconnection network. Int. j. Electronics Electrical Eng., 20: 335-345.
4. Bansal P.K., R.C. Joshi, K. Singh and G.P. Siroha, 1991. Fault-tolerant augmented baseline multistage interconnection network. Proceeding of the 10th International Conference on EC3-Energy, Computer, Communication and Control Systems, Aug.28-30,pp200-204.
http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnum ber=729643.
5. Bhuyan Laxmi N., Yang Qing and P. Agrawal Dharma, 1993. Performance of multiprocessor interconnection networks. IEEE Comput., 22: 25-37.
6. Duato Jose, Yalamanchili Sudhakar and Ni Lionel, 2003. Interconnection Networks: An Engineering approach, published by Elsevier Sc., pp. 23-29.
7. Lubazewski M. and Coutois B., 1998. A reliable fail-safe system, parallel and distributed systems. IEEE Comput. Soc., 47: 236-241.
8. Nitin Chanderwal, 2006. On analytic bounds of regular and irregular Fault-tolerant Multistage Interconnection Networks. Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA), June 26-29, pp. 221-226.
9. Sadawarti Harsh and P.K. Bansal, 2007. Fault tolerant irregular augmented shuffle network. Proceedings of the 2007 Annual Conference WSEAS International Conference on Computer Engineering and Applications, WSEAS, Gold Coast, Australia, Jan. 17-19, pp: 7$13 \mathrm{http}: / /$ portal.acm.org/citation.cfm?id=1348260.
10. Sengupta J. and P.K. Bansal, 2000. Reliabilty and performance measures of regular and irregular multi-stage interconnection networks. Interational Conference IEEE TENCON, pp: 531-536.
11. Sengupta J. and P.K. Bansal, 1999. Performance analysis of regular and irregular dynamic MINs. Proceeding of the $10^{\text {th }}$ International Conference IEEE Region 10 TENCON 99, Sep. 15-17,pp:427430. Doi: 10.1109/TENCON.1999.818442.
12. Sharma Sandeep, K.S. Kalhon, P.K. Bansal and Singh Kawaljeet, 2008. Improved irregular augmented shuffle exchange multistage interconnection network. Int. J. Comput. Sci. Security, 2: 28-33.
13. Sharma Sandeep, K.S. Kalhon, P.K. Bansal and Singh Kawaljeet, 2008. Irregular class of multistage interconnection networks in parallel processing. Int. J. Comput. Sci., 4: 220-224.
