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An Analysis of Interleaved Boost Converter with LC Coupled Enhanced Soft Switching

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ABSTRACT

An enhanced soft switching technique for an interleaved boost converter with Zero Current Switching (ZCS) and Zero Voltage Switching (ZVS) during OFF and ON conditions of the main switches, that can drive large loads operated in duty cycle greater than 0.5 is proposed in this study. In this topology, auxiliary circuit is composed of resonant tank which is used to decrease the voltage stress on the main switches and a coupling capacitor is added additionally with minimum resonance which in-turn increases the life of operation of the converter. In this model, faster switching and suitable impedance matching is achieved with reduction in auxiliary circuit reactance that has contributed much increase in the overall performance. Coupled inductor in the boosting stage helps higher current sharing between the switches. The overall ripple and Total harmonics distortions are reduced in this technique without sacrificing the performance and efficiency of the converter. A simulation module constructed using "MATLAB Simulink" illustrates the better results of the proposed converter.

Keywords: Interleaved Boost Converter, Zero Voltage Switching, Zero Current Switching, Duty Cycle

1. INTRODUCTION

The boost converter is a popular choice for most power electronic systems to serve as a pre-regulator, due to advantages of simplicity and high performance (Pan *et al*., 2009). However, as the power rating increase, it is often required to associate converters in series or in parallel. In high-power applications, interleaving of two boost converters is very often employed to improve performance and to reduce the size (Gallo *et al*., 2010). Because interleaving effectively doubles the switching frequency and also partially cancels the input and output ripples, the size of the energy-storage inductors and differential-mode EMI filter in interleaved implementations can be reduced (Jang and Jovanovic, 2007). Interleaving reduces the output capacitor ripple current as a function of duty cycle. As the duty cycle approaches 0, 50 and 100% duty cycle, the sum of two diode currents approaches dc. At these points, the output capacitor only has to filter the inductor ripple current. It can be shown that by applying different duty cycles to the two phases of an interleaved boost converter according to voltage- second balance, their voltage gain will be different. The phase with larger duty cycle may have large voltage gain and operate in Continuous Inductor Current Mode (CICM), while the other will then automatically operate in Discontinuous Inductor Current Mode (DICM). Under this condition, any further additional loading current will be taken up by the phase CICM operation (Wang *et al*., 2008). Hence the analysis of the converter operated in duty cycle greater than 50% is an efficient approach in interleaved boost converters.

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The AC mains utility supply ideally is supposed to be cleaned and free from high voltage spikes and current harmonics in order to ensure good quality and efficient power system harmonics to electronics equipment. But in practical condition the ripples are inevitable, which needs to be minimized (Daut *et al*., 2006). Various ongoing research proposals are focused with some limitation as follows.

To reach the smooth soft switching, the circuits proposed require more complex auxiliary circuits which totally increase the conduction loss (Stein *et al*., 2002; Hsieh *et al*., 2009). Due to extra inductor, the auxiliary unit is complex, even the main switches are ZCS and the auxiliary switches are ZVS. The main switches are ZCS at the turn-on transition, while in turn off the switching is hard (Stein *et al*., 2002). A better soft switching circuit is proposed, but the converter works in discontinuous mode with duty cycle less than 50% (Yao *et al*., 2007). Even after analyzing with duty cycle more than 50%, the number of switching phases and switching timing is high due to increased auxiliary resonance and voltage stress to the auxiliary switch (Chen *et al*., 2012). The higher switching frequency may cause the higher switching losses, higher Electro-Magnetic Interference (EMI) and the lower overall efficiency. The use of soft-switching techniques in converter can contribute to reduce them (Felix and Kumar, 2012).

In this study, a soft switching technique for an interleaved boost converter with Zero Current Switching (ZCS) and Zero Voltage Switching (ZVS) for the main switches, which is operated in duty cycle greater than 50% with wide range of operating load, is proposed. In this topology, the voltage stress on the main switches is shared by the resonant tank composed of a resonant capacitor and inductor forming an effective auxiliary circuit. To increase the durability of the switch used, a coupling capacitor is added additionally with minimum resonance. Faster switching and suitable impedance matching is achieved with reduction in auxiliary circuit reactance which has increased the overall performance. Better current sharing between the switches is obtained by coupling the boost inductors. The overall ripple and Total harmonics distortions are reduced with higher efficiency of the converter. The forth coming sections will reveal the effectiveness of the enhanced converter.

2. MATERIALS AND METHODS

2.1. Design and Analysis

For the case analysis, the circuit is analysed in Continuous Conduction Mode (CCM) with various load ranges having different duty cycle. The Proposed interleaved Boost Converter with LC coupled Soft Switching is shown in **Fig. 1**. It utilizes the interleaved boost converter topology and applies enhanced soft switching methodology where the resonant tank itself triggers the switches for extreme condition. The resonant tank is composed of Resonant Capacitor Crc and Resonant Inductor L_{rc} which in-turn act as a control circuit for the auxiliary switch S_{ax}, that is responsible for ZVS and ZCS function.

2.2. Principle of Operation

The circuit is operated in fundamental mode with duty cycle D which is exact symmetrical in function. The circuit is analysed with certain assumptions to simplify the circuit analysis which are listed as:

- All switches and diodes are assumed to be in practical condition with an exponential decay α in the computation for theoretical analysis
- Idealizing the input and output reactance
- The two boost inductors are coupled
- Same duty cycles ($D_1 = D_2$) for the main switches S_{s1} and S_{s2}

The flow of current in initial stages through the boost inductor has an effect of interference which results in addition of ripples. Thus, for the initial input current to be clear from input ripple, a guard is introduced, which is a magnetic couple by a ferrite core which has high permittivity and hence the coupling is more effective.

Boost inductors B_{L1} and B_{L2} is energized by the magnetic flow across the inductor causing fluctuation in the input current. It is minimized by placing the iron core between the coils which looks like a transformer arrangement. Thus the flow of current is regulated by the magnetic coupling across the inductors.

The mutual inductance exerted by both the boost inductor is given by Equation 1:

$$L_m = (u_r \sqrt{L_1 L_2})K \quad (1)$$

where, μ_r and K are Permittivity of the core and coupling co-efficient respectively.

According to the circuit theory, the coupled inductor can be realized with an uncoupled inductor which needs an additional inductor for coupling. There by Equation 2 and 3:

$$L_1^{'} = L_1 - L_m \quad (2)$$

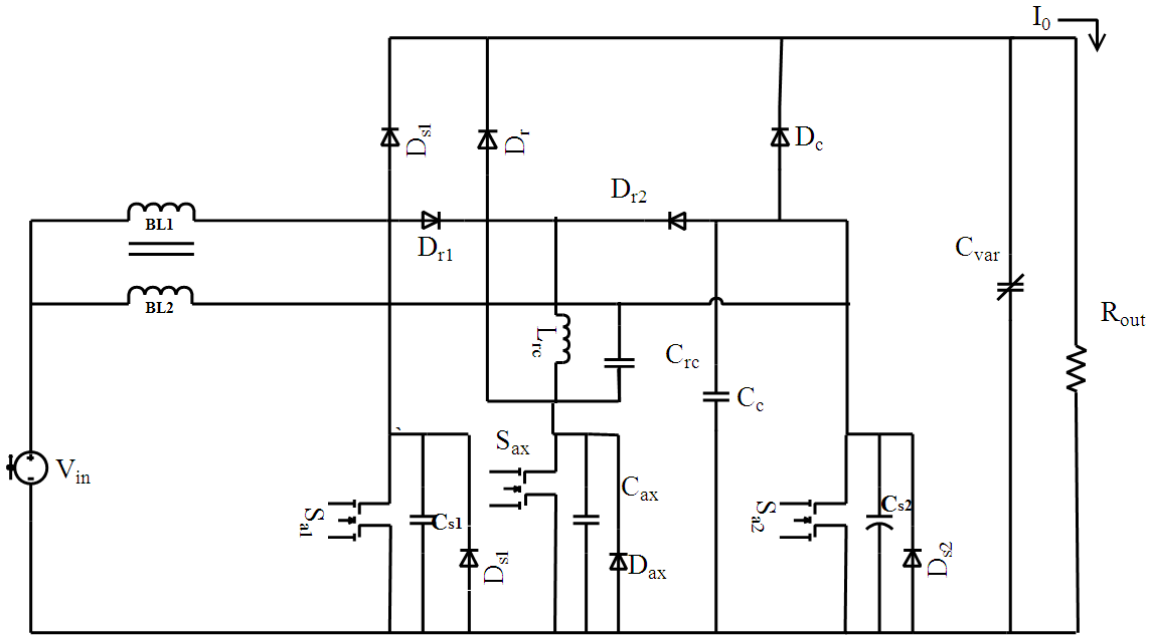


Fig. 1. Proposed interleaved boost converter with LC coupled soft switching

$$L_2^{'} = L_2 - L_m \quad (3)$$

where, $L_2^{'}$ and $L_1^{'}$ are considered to be leakage inductances which has major influence over the input current ripple. By regulating the coupling coefficient, the amount of ripples in the input current can be controlled. On the other hand, the output from the inductor is given by the expression which depends only on the leakage inductance Equation 4 and 5:

$$\frac{d_i L_1}{dt} = \frac{-v_o}{L_1^{'} + L_m} = \frac{v_o}{L_1} \quad (4)$$

$$\frac{d_i L_2}{dt} = \frac{-v_o}{L_1^{'} + L_2^{'}} \quad (5)$$

The overall current in the converter is given by the Equation (6), which is the hypotenuses cosine function of the capacitance:

$$I = \int_0^{t6} -K\left(1 - \cosh\left[\frac{c_r + c_{sh}}{c_{sh} + c_r}\right]\right)dt \quad (6)$$

The significance of the equation is that overall effectiveness of current sharing of the converter is predetermined from the inductor current. Flow of current through the two switches is calculated by the following expressions Equation 7 and 8:

$$I_1 = \sum_{s_{s1}=ON} \frac{v_{in}(1 - D_1 + D_{r2} + 2D_{rc})T}{L_1 L_2} \quad (7)$$

$$I_2 = \sum_{s_{s2}=ON} \frac{v_{in}}{1 - (D_r + D_{rc} + 2D_{rv})} \quad (8)$$

The overall cycle time is of the inductor output current with or without ripple and it can be expressed in the time of propagation of current in inductor, which is usually specified as a function of line frequency of input (i.e., Indian standards, 50 Hz) Equation 9:

$$T_{Cycle} = 2.37 \log_2 t_p \quad (9)$$

In this consideration of the switch S_{s1}, the total power applied to the auxiliary switch is given by the expression (10). The resistance in the parasitic (R) elements contributes for the maximum power usage in the switch Equation 10-12:

$$P_{s1} = 2(I(t_p))^2 R \quad (10)$$

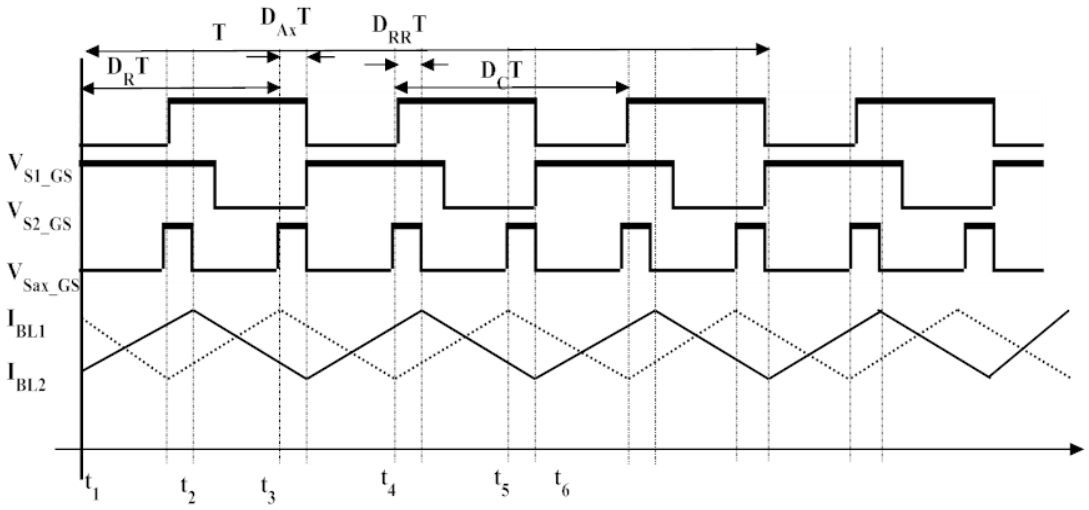


Fig. 2. Related switches driving signal D>50%

$$l(t_p)\int_0^{t_r} l_l(t)\,dt \tag{11}$$

$$I(t_p)=\int_0^{t_r}\left[\begin{array}{c}-V_o\sqrt{\frac{C_1C_s}{L_r(C+C_c)}}\sinh\sqrt{\frac{C_r+C_{ax}}{L_rC_1C_{ax}}}+\\ \frac{I_{L2}C_{ax}}{C_1C_{ax}}1+\cos\left(\frac{C_1+C_r}{C_1C_r}\right)t\end{array}\right]dt \tag{12}$$

The overall output current $I(t_p)$ in the converter is calculated as the integral of inductor current. The current purely depends on the resonant circuit of the device in use.

It is an inevitable fact that, in practical conditions, it is not possible to produce the duty cycle exactly at 50%., hence the design is analysed for two different modes of operation viz duty cycle (D) lesser and greater than 50%.

2.3. Operational Analysis when Duty Cycle is Greater than 50%

In this analysis, there are 12 operational modules which comprise of a complete cycle. Here, analysis is done only on 6 modes which are related to main switch S_{S1}. The operating modes of the circuit for duty cycle greater than 50% is shown in **Fig. 2 and 3** shows the related wave forms under same condition. **Fig. 4a-f** shows the active stages of the converter during operation.

Stage I [t_0 –t_1]

In this stage, due to the pre-excitation in duty cycle, all the switches (S_{s1}, S_{s2}, S_{ax}) are active and the rectifier diodes D_{r1}, D_{r2} and clamped diode D_r are turned off. Here the main switch current I_{s1} and I_{s2} are less than previous mode. The main switch S_{s2} achieves ZCS at time $t_1 = t_0$ Equation 13:

$$t_{01} = (D - t_{07})T - (D_1 - 0.5)T \tag{13}$$

Based on the equation at Stage 3 in D<50%.

The inductor current between the intervals is given by Equation 14:

$$I_{Lrc}(t) = i_{BL2}(t_a) + \frac{v_0}{\sqrt{\frac{L_{rc}}{C_{s2}+C_{ax}}}} \geq I_{Lin} \tag{14}$$

Stage II [t_1–t_2]

Here, the energy stored in the resonant circuit [L_{rc},C_{rc}] is transferred to the output load by a clamped diode D_r. This happens because auxiliary switch voltage attains zero. The flo‹v of current from resonant circuit I_{rc} is equal to the total output current I_0 which is equal to boost inductor current I_{BL1} (t) Equation 15:

$$I_{rc} = I_0 = I_{BL1}(t) = K\left[\begin{array}{c}I_{in} - \cosh\left[\frac{C_{ax}+C_{sh}}{C_{sh}C_{ax}}\right]\\ \left(\frac{L_B - L_{rc}}{L_BL_{rc}}\right)\end{array}\right] \tag{15}$$

The overall execution of stage 2 is based on the LC resonant that produces damped oscillation in LC network which is supported by an input voltage that makes the system to produce sustained output.

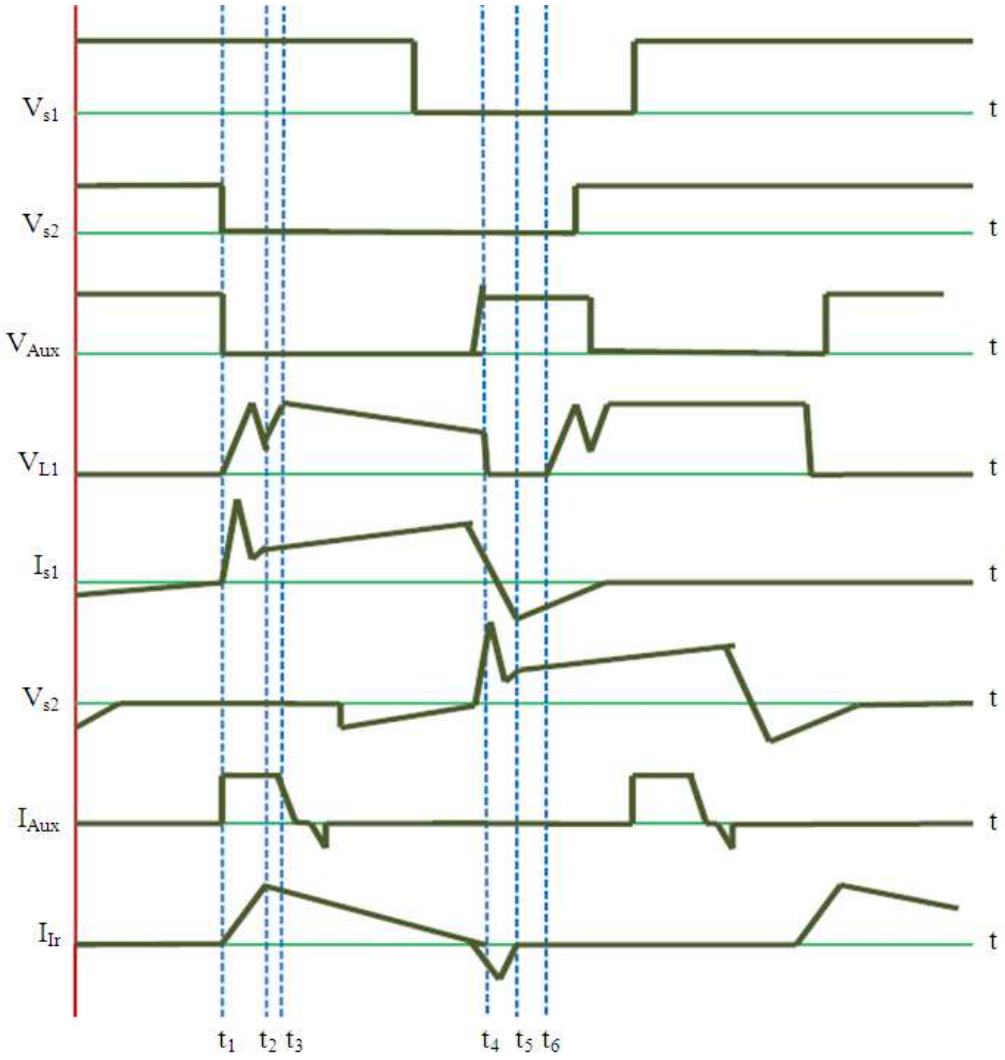


Fig. 3. Stages of the switches when it is operated with duty cycle greater than 50%

Stage III [t_2–t_3]

At this stage, the damped diode D_r is turned off. The energy stored in boost inductor BL_1 and the parasitic capacitor C_{s1} is transferred to resonant circuit and hence the rectifier diode D_{r2} is turned on. When the main switch voltage V_{s1} and resonant capacitor C_{rc} increases to V_0 at $t = t_3$ Equation 16-18:

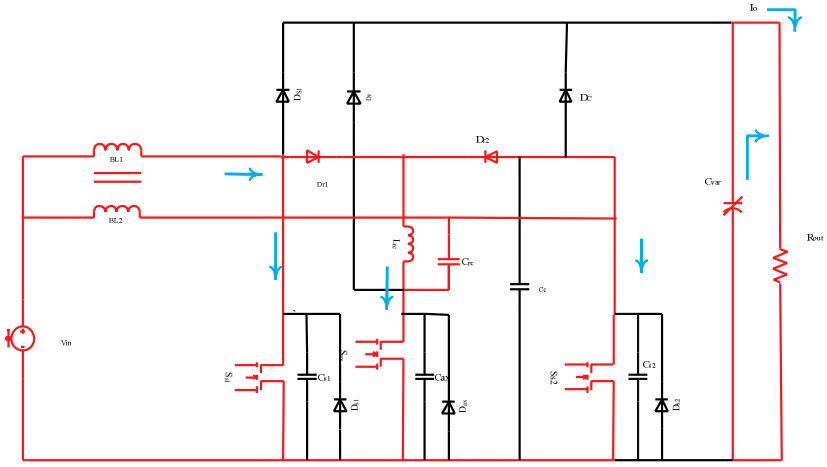
$$t_{23} = t_{01} + t_{12}$$

$$t_{23} = \left[L_{B1}\frac{I_{Lin}}{V_0} + \frac{\pi}{2} I_{in}\sqrt{L_{rc}(C_{s1} + C_{s2} + C_0)} \right] \quad (16)$$

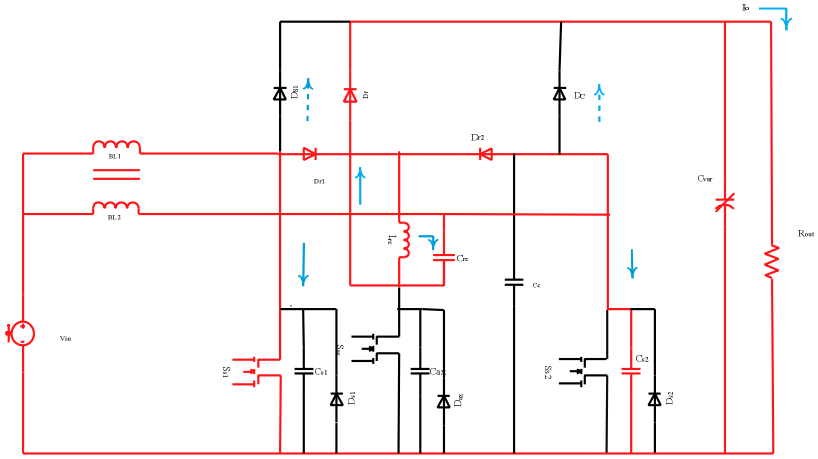
$$I_{Lr}(t) = \left[-V_0\sqrt{\frac{CC_{rc}}{L_{rc}(C + C_{rc})}}\sin\sqrt{\frac{C + C_{rc}}{CC_{rc}}}t + \frac{I_{L2}C_{rc}}{C + C_{rc}} X\left(1 - \cos\left(\sqrt{\frac{C + C_{2\gamma}}{L_{2\gamma}C}}t\right)\right) \right] \quad (17)$$

$$t_{23} = \pi\sqrt{\frac{L_r C_{rc}}{L_{rc}(C + C_{rc})}}t \quad (18)$$

The parasitic capacitor C_{ax} of the auxiliary switch is given linearly by I_{BL2}-I_{rc} to V_0.



(a)



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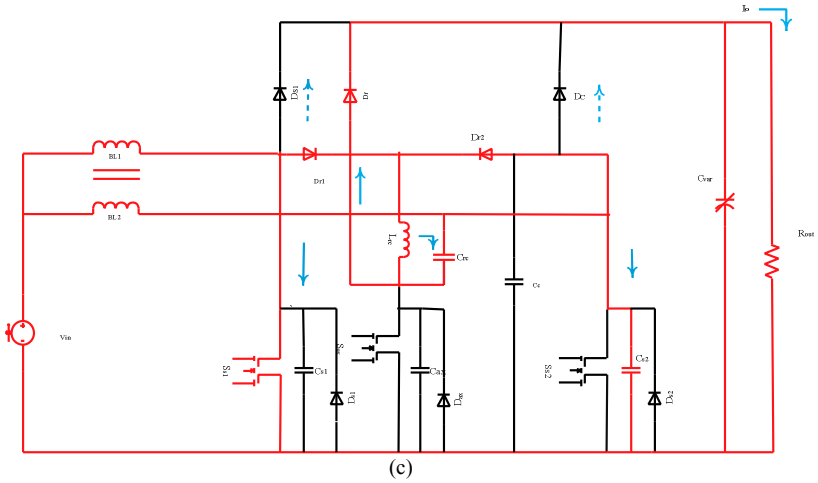

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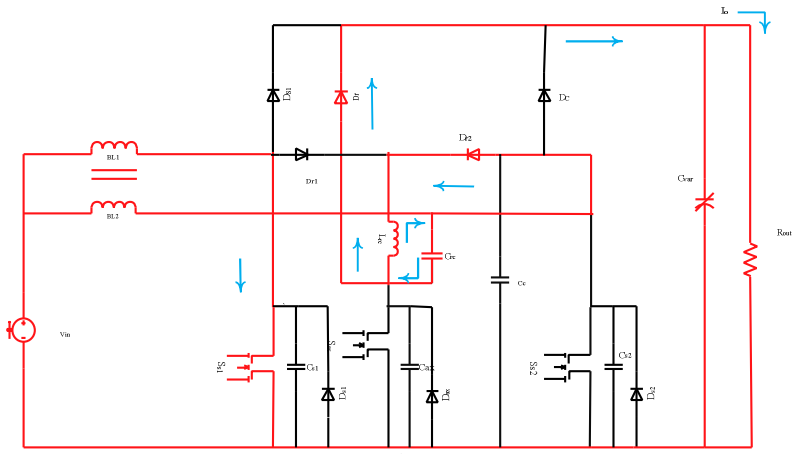
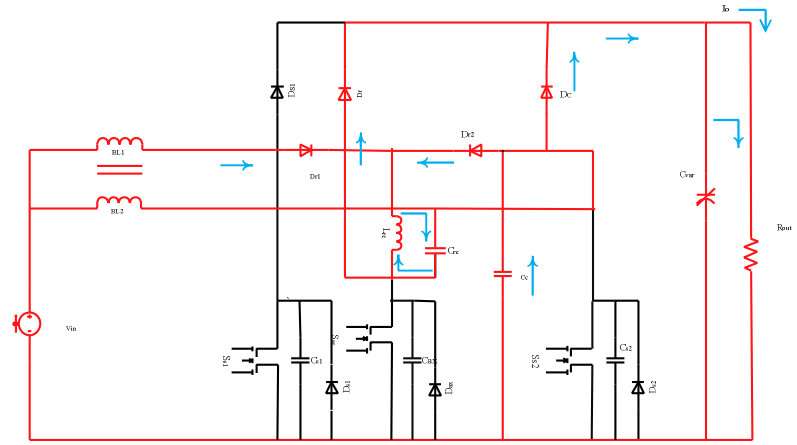
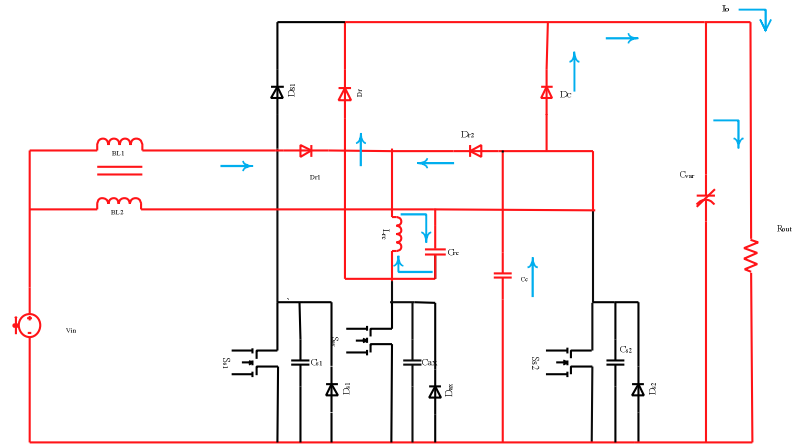


(d)



(e)



(f)

Fig. 4. Operating modules when the duty cycle is greater than 50% (a) Stage I (t0-t1), (b) Stage II (t1-t2), (c) Stage III (t2-t3), (d) Stage IV (t3-t4), (e) Stage V (t4-t5), (f) Stage VI (t5-t6)

Stage IV [t_3-t_4]

In this stage, at t_4 the clamped diode D_r is turned ON. The energy stored is the inductor L_{rc} is transferred to output V_o through clamped diode D_r and the Switch S_{S2} turn-on has no effect on the main switch S_{S1}.

In this the time, it is necessary to consider an intermediate time which is given Equation 19 and 20:

$$t_{34} \geq t_{23} + \frac{\pi}{2}(t_0) \qquad D \geq 0 \tag{19}$$

$$t_{34} = \frac{\pi}{2}\omega_D \quad \omega = \frac{3}{2}\pi\sqrt{L_{rc}C_{rc}}$$
$$\omega_D = 3\frac{\pi}{2}\sqrt{L_{rc}(C_{s1}+C_{s2}+C_c)} \tag{20}$$

So the excitation current I_{Lin} (t_n) is given is terms of time constrain Equation 21:

$$I_{Lin}(t) \approx I_{Lin}(t_3) = \left[\frac{i_{rcV0}^{(t_3)} +}{\sqrt{L_{rc}(C_{s1}+C_{s2}+C_c)}}\right] \geq I_0 \tag{21}$$

Stage V [t_4-t_5]

In this stage, both main and auxiliary switches are turned OFF. The stored energy in LC network is discharged to the load via D_r which is a clamped diode and that will act as a bypass for the current flow. Now the input current charges the parasitic capacitance in the switches. The resonant current continues to increase to the peak value and the main switch voltage C_{s1} decrease to zero, because of the resonance, among elements, turns the switch S_{S2} to be in ON condition Equation 22 and 23:

$$t_5 - t_3 = \frac{L_{rc}}{V_0}\left(i_{rc}(t_a) + \frac{V_0}{z_0}\right) \tag{22}$$

$$t_5 - t_3 = \frac{L_{rc}}{V_0}\left(i_{rc}(t_a) + \frac{v_0}{\frac{L_{rc}}{(C_{s1}+C_{rc})}}\right) \tag{23}$$

At this stage, all the voltages tend to equal. V_{rc} (t_5) = V_{c1} (t_5) = V_{s2} (t_5) = V_{cc} (t_5) = V Equation 24:

$$V = \frac{1}{(C_{s1}+C_{s2}+C_r+C_{cc})}\int_{t_6}^{t_7}(I_{Lin}+i_{Lrc}(t))dt \tag{24}$$

Now at the end of this stage, the charged inductor helps the rectifier diode to turn ON.

Stage VI [t_5–t_6]

When the resonant capacitor voltage V_{cr} and the main switch voltage V_{s2} are equal to zero, the body diode D_{S2} of S_{S2} is turned ON. The time should be a fraction of normal operational time of stages. So in this stage one main switch S_{S1} achieves ZCS and other Main Switch S_{S2} achieves ZVS Equation 25:

$$t_6 = \frac{T}{2} - \frac{(t_{01}+t_{12}+T_{23})}{L_{rc}C}V_0 \tag{25}$$

2.4. Voltage Ratio

Boost inductor current i_{BL1} when switch is active in duty cycle greater than 50%, where active stages are (t_{01},t_{23},t_{45}) Equation 26-28:

$$\sum_{s1=ON} i_{L1} = \frac{v_{in}}{L_1}(t_{01}+t_{23}+t_{45}) \tag{26}$$

$$= \frac{v_{in}}{L_1}(D_1^{'} + 0.5D_r + 2D_{rc})T \tag{27}$$

$$= \frac{V_{in}}{L_1}(D_r + 2D_{rc})T \tag{28}$$

Boost inductor current i_{BL1} when switch is active in duty cycle greater than 50%, where active stages are (t_{12}, t_{34}, t_{56}).

Total time for switch to be in ON is T-(t_{12}+t_{34}+t_{56}) Equation 29 and 30:

$$\sum_{s1=OFF} i_{L1} = \frac{V_{in}}{L_1}(T-(t_{12}+t_{34}+t_{56})) \tag{29}$$

$$\sum_{s1=OFF} i_{L1} = \frac{[V_{in}-V_{out}]}{L_1}(1-(D_r+2D_{rc}))T \tag{30}$$

Voltage conversion ratio is given by Equation 31:

$$\frac{V_{out}}{V_{in}} = \frac{1}{(1-(D_r+2D_{rc}))} \tag{31}$$

2.5. Simulation Design and Analysis

2.5.1. Converter Specification

The switching frequency f_s = 50 Hz, the output voltage V_0 = 440V and the range of output power P_{out} are 200W-800W. The range of operating voltages 150V-220V.

2.6. Estimation of Boost Inductors and Output Capacitor

To support wide range of load a variable capacitor is used to provide impedance matching between the levels. The range of output capacitance is 200-700 μF most preferably above 400 μF. The boost inductors B_{L1} and B_{L2} are designed to operate in CCM. The design consideration of the parameters are given by:

- Calculation of inductance-Duty cycle greater than 50% Equation 32:

$$B_{L1\min} = \frac{(D_r + D_{rc})[D_1 - (D_r + D_{rc})^2 R_{max}]}{f_s} \quad (32)$$

$$B_{L1} = 21\,\mu H$$

Thus average inductance for both the boost inductor is given by B_{L1} and B_{L2} iws 23 μH.

2.7. Estimation of Resonant Capacitor and Coupling Capacitor

Resonant capacitor plays an important role in all aspects of switching, energy storage, impedance matching and load driving so the design of resonant capacitor enhances the overall performance of the converter. The total reactance of the system is the sum of reactance from capacitor and inductor which is equal to the overall energy stored in the system:

$$Q = X_L + \frac{1}{X_C}$$

where, X_L and $\frac{1}{x_C}$ are reactance of inductor and capacitor respectively.

Consider the charge and equivalent energy charge per storage in resonant tank. The operating frequency of the tank circuit is given by 50Hz, so the calculation of resonant capacitor is obtained from (33) by substituting known values Equation 33:

$$\frac{1}{f_s} = \frac{\pi}{2}\sqrt{L_r(C_{S1} + C_{S2} + C_c + C_r)} \quad (33)$$

By simplification with the known values of maximum allowed parasitic capacitance in MOSFET switches, the coupling capacitance and resonant capacitance is given as 1.5 μF and 2.5 μF respectively.

2.8. Estimation of Switching Time

Switching time of the converter is controlled by the resonant and parasitic elements by analyzing those elements which will give necessary time constraint for soft switching.

Table 1. Parameters and components of the converter

Input voltage	180-240V
Duty cycle	>50%, for simulation 60%
Output voltage	440V
Output current	0.5A-1.45A
Output power	200-800W
Switching frequency	50Hz
Boost_L_1&Boost_L_2	23μH and Ferrite core $\mu_r = 10$
Output capacitor	200-700 μF
Resonant inductor	5 μF
Resonant capacitor	1.5 pF
Coupling capacitor	2.5 pF

2.9. Design of Arrival Time of ZVS Condition

When time taken by the switch S_{S1} to achieve ZVS, the voltage across the source to drain must be zero. The same is achieved in stage 5 for mode D>50%. The minimum time considered for the arrival of ZVS is given by.

For stage 5 (D > 50%), the calculation of ZVS arrival time is given as Equation 34:

$$D_{S1} > t_{45} = \frac{\pi\sqrt{L_{rc}(C_{S2} + C_c + C_{rc})}}{2} = \frac{3.14 \times \sqrt{5\mu \times 785p}}{2} = 197.00\text{ns} \quad (34)$$

2.10. Design of Arrival Time of ZCS Condition

Time at which the switch S_{S2} achieve ZCS is in stage 6 for mode D>50%. The minimum time considered for the arrival of ZCS is given by the resonant inductor current.

In stage 6 (D >50%), the calculation of ZVS arrival time is given as Equation 35 and 36:

$$i_{Lrc}(t_6) = I_{BL2}(t_a) + \frac{V_0}{Z_1} = 7.15A > I_{in} \quad (35)$$

$$D_{S1} > t_{5a} + t_{a6} = \left[L_{rc}\frac{I_o}{V_o} + \frac{\pi\sqrt{L_{rc}(C_{S2} + C_c + C_{rc})}}{2} \right] = 225\text{ns} \quad (36)$$

Thus, the design can give the Maximum Duty time of soft switching condition with the above constraints. All the above parameter values are tabulated in **Table 1**.

2.11. Parametric Analysis of the Circuit

The interleaving technique in power convertor is simulated with desired specification of ZCS and ZVS. Furthermore for better understanding, Total Harmonic Distortion (THD), the efficiency, operational range, gain, stabilizing the duty cycle and reverse recovery loss are to be calculated. The overall mathematical analysis is focused on such qualities for easier optimization of the circuit.

2.12. Total Harmonic Distortion (THD)

In this study, the harmonics of interleaved boost converter is analyzed from 3rd harmonic to 13th harmonic where the maximum harmonics can be obtained. Basically total harmonics is the Root Mean Square (RMS) value of the total harmonics of the signal, by the RMS value of its fundamental signal. Let the Fourier co-efficient are Equation 37:

$$b_n = \frac{4E}{n\pi}\cos(na) \tag{37}$$

For 3rd harmonic, the change of angle in the wave is given by a = 30° then the harmonic from 3rd is given by the Mathematical Induction Equation 38:

$$THD = \sqrt{\frac{2\pi(\pi - 2d) - 16\cos^2 a}{4\cos(a)}} \tag{38}$$

By changing the Fourier's co-efficient for two switches Equation 39:

$$\begin{aligned} &b_n = \frac{4E}{n\pi}(1 - \cos(na_1) + \cos(na_2)) \\ &\text{where, } n = 1,3,5 \\ &THD = \frac{\sqrt{\pi\left(\frac{\pi}{2} + a_1 a_2\right) - (1 - \cos(a_1) + \cos(a_2)^2)}}{1 - \cos(a_1) + \cos(a_2)} \end{aligned} \tag{39}$$

By Fourier transform Equation 40:

$$X(n) = a_0 + \sum_{n=1}^{N-1}\begin{bmatrix} a_n \sin(2\pi fn) + \\ b_n \cos(2\pi fn) \end{bmatrix} \tag{40}$$

By harmonic on stages of 3, 4, 5, 6, 7 is given by.

The angular change α is given for harmonics is Equation 41:

$$\left.\begin{aligned} \cos(a_2) + \cos(a_2) + \cos(a_2) + \cos(a_4) &= 4 \\ \cos(5a_1) + \cos(5a_2) + \cos(5a_2) + \cos(5a_4) &= 0 \\ \cos(7a_2) + \cos(7a_2) + \cos(7a_2) + \cos(7a_4) &= 0 \\ c0s(11a_2) + \cos(11a_2) + \cos(11a_2) + \cos(11a_4) &= 0 \\ \cos(13a_2) + \cos(13a_2) + \cos 13(a_2) + \cos(13a_4) &= 0 \end{aligned}\right\} \tag{41}$$

By applying Newton-Raphson iterative method Equation 42:

$$\begin{aligned} &a_1 = 6.6°, a_2 = 18.9°, a_3 = 27.2°, \\ &a_4 = 45.3°, a_5 = 54.6° \\ &THD = \frac{\sqrt{\frac{\pi^2 p^2}{n}} + \frac{\pi}{4}\sum(2i+1)a_{i+1} - (\sum_{i=1}^{p} CO3(a_1)^2)}{\sum_{i=1}^{p} CO3(a_i)} \end{aligned} \tag{42}$$

On the basic calculation for the iterative equations, the maximum THD is 7.93%.

2.13. Current Sharing

The current sharing in parallel path is a major design problem, which is minimized by using a coupled inductor in input stage. The magnetic interference on the adjacent path couples the flow of current and so the current sharing between the parallel conductors will turn to be effective. Average current that is shared by the switches are equal i.e., $\frac{v_0}{z_{out} - (D_r + D_{rc} + 2D_{rv})}$.

Thus the current from an inductor B_{L1} is controlled by both the inductor, so maximum sharing of current can be easily achieved. This shows that the current flowing through the switches is equal to each other. The circuit is symmetrical and hence the expressions for the flow of current through the paths are meant to be equal. From the above, the average Current Shared by Inductors I_{L1} and I_{L1} is manipulated to be 3.5A.

2.14. Diode Conduction and Reverse Recovery Losses

The recovery current in terms of charge and recovery time enable the calculation of the loss are found to be simple Equation 43 and 44:

$$I_{RR} = \frac{2Q_{RR}}{t_{rr}} \tag{43}$$

$$t_{rr} = \frac{2Q_{RR}}{di/dt} \tag{44}$$

Total power loss in conduction of a diode is given from the RMS values of the conduction. This loss can only be minimized because there is power dissipation in conduction due to the recombination of electrons Equation 45:

$$P_{cdb} = \frac{4 * \sqrt{2} * P_0 * v_F}{\pi ** V_{rms}} \tag{45}$$

In switching the operation of diode for rectification of input the loss associated with the clamped diode is given as a function of change in phase angle and with the total charge recovery of the diode Equation 46:

$$P_{SDB}(V_i, \theta) = Q_{rr} * V_i * \sin\theta * f \quad (46)$$

Here θ, angle of recovery current Equation 47:

$$I_{CS1} = \frac{\sqrt{2} - P_0 - \sin\theta}{*V_{rms}} \quad (47)$$

Power dissipation for a complete cycle of single stage boosting is given from the total time (T) to the reverse recovery time (t_{rr}) Equation 48:

$$P_{cycle} = \left(\frac{V}{T} * t_{rr}\right) * \left(\frac{I}{T} * t_{rr} + I\right) \quad (48)$$

From the above calculation the total switching loss in a converter is given by Equation 49:

$$P_s = f_s * (V_{ef} + V_0) * Q_{rr} \quad (49)$$

Finally, the reverse recovery loss of overall system including 8 diodes and 3 switches is 12.96 Watts which is just 2.16% of total power.

3. RESULTS AND DISCUSSION

The operation of the converter under the various load from 200 to 800W with the duty cycle greater than 50% are shown below. Based on the design consideration and required conditions, the proposed interleaved boost converter with both ZVS and ZCS characteristics is built and it is shown in concerned places with proper indication. The simulated output waveforms (**Fig. 5-6**) of the proposed circuit are obtained with an input voltage of 150V and the load current of ~0.6A. While verifying the output of both the switches S_{S1} and S_{S2}, it will be same, as the circuit is symmetrical. The proposed method has a designed switch with a practical decay constant (α) which is dependent factor on temperature, working life span, range of conductivity and various physical factors.

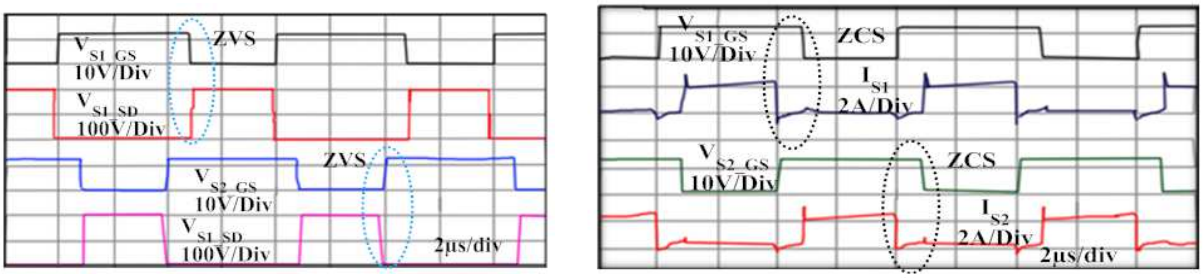


Fig. 5. Simulation waveforms of the main switches S_{S1}, S_{S2} (a) (b) ZVS and ZCS operation while operating in duty cycle above 50% with load current 0.55A

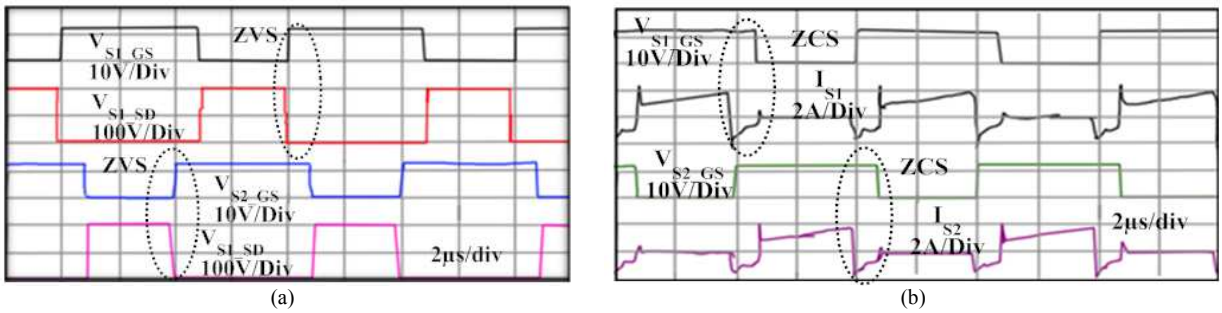


Fig. 6. Simulation waveforms of the main switches S_{S1}, S_{S2} (a) (b) ZVS and ZCS operation while operating in duty cycle above 50% with load current 1.45A

Table 2. Comparison of various parameters

Parameters	Lee *et al*. (2000)	Stein *et al*. (2002)	Yao *et al*. (2007)	Chen *et al*. (2012)	Proposed converter
Current Sharing by switches	*Not exactly equal	*Not exactly equal	*Nearly equal	*Nearly equal	3.5A (equal)
THD	-	-	-	-	7.93%
Reverse recovery loss	-	-	-	-	2.16%
Time of ZVS	*In range of ms	*In range of ms	*In range of ms	211ns	197ns
Time of ZCS	*In range of ms	*In range of ms	*In range of ms	249 ns	225ns
Efficiency	94.20%	95.90%	95%	95.50%	97.80%

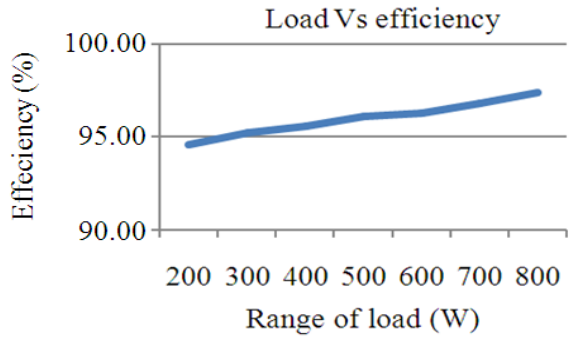


Fig. 7. Efficiency measurement

The efficiency measurement for various loads is shown in **Fig. 7**, which shows the effectiveness of the proposed converter. Various parameters are tabulated in **Table 2** which compares the performance of existing converters and proposed converter. The switching timing of the proposed converter indicates the fast switching transition of the circuit when compared with existing topologies. Further, the results shows that the proposed converter can be implemented with better power factor for the practical applications like Solar System, PV Panel, Grid Systems, Green Power System and Semiconductor Industries.

4. CONCLUSION

An enhanced soft switching technique for an interleaved boost converter with Zero Current Switching (ZCS) and Zero Voltage Switching (ZVS) for the main switches operated in duty cycle greater than 50% is proposed in this study. The converter can drive wide range of load with higher efficiency. From this topology, decreased voltage stress of the main switches, faster switching, suitable impedance matching, better THD, reduced ripples, reduced reverse recovery loss and conduction loss, equal current sharing and better overall efficiency is achieved, which effectively reveal the performance of the proposed converter.

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